Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method for processing an instruction within a processor, wherein the processor processes a plurality of types of interruptions, and wherein the processor comprises a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are active within the processor, the method comprising:

executing an instruction within the processor;

receiving an interruption signal by the processor;

indicating whether the trap mode is active or inactive using a trap mode field within the processor, wherein a first trap mode field indicates that a single-step trap mode is active and wherein a second trap mode field indicates that a taken-branch trap mode is active;

in response to receiving the interruption signal, determining whether a trap mode is to remain active during interruption processing;

in response to a determination that the trap mode is to be deactivated during interruption processing, deactivating the trap mode; and

invoking an interruption handler to perform in interruption processing for the received interruption signal.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Original) The method of claim 1 further comprising:

indicating whether a trap mode is to remain active during interruption processing using a trap mode conditioning field within the processor.

6. (Original) The method of claim 5 wherein a first trap mode conditioning field conditions activity of a single-step trap mode.

7. (Original) The method of claim 5 wherein a second trap mode conditioning field conditions activity of a taken-branch trap mode.

8. (Original) The method of claim 1 further comprising:
performing a trace operation prior to deactivating the trap mode.

9. (Original) The method of claim 1 further comprising:
reactivating the trap mode after interruption processing.

10. (Original) The method of claim 9 further comprising:
performing a trace operation after reactivating the trap mode.

11-30. (Canceled)

31. (Previously Presented) The method of claim 1 further comprising:
determining the manner in which contention is resolved between trap mode processing and interruption processing based on a trap mode conditioning field of the processor status register.

32. (Previously Presented) The method of claim 31 wherein a processor does not preserve the trap mode in any manner when an interruption occurs.

33. (Previously Presented) The method of claim 31 wherein the processor suspends the trap mode when an interruption occurs.

34. (Previously Presented) The method of claim 31 wherein the processor preserves the trap mode when an interruption occurs.

35. (Previously Presented) The method of claim 31 wherein the trap handler immediately relinquishes execution control back to the interruption handler without performing any trace operations.

36. (Previously Presented) The method of claim 31 wherein the trap handler generates a trace record when the trap handler is first invoked after the interruption handler has been entered, thereby providing a trace record at the start of the exception processing for the interruption.

37. (Previously Presented) The method of claim 31 wherein the trap handler generates a trace record when the trap handler is invoked after the interruption handler has completed its processing operations, thereby providing a trace record at the end of the exception processing for the interruption.